

BiSS Interface Application Note #2

Recommendations For Communication Setup

1. General

Parameter	Symbol	Min	Max
Maximum Cable Length (twisted-pair cable and RS422 drivers)		-	1200 m
Clock Frequency Sensor Mode	$1/T_{MAS}$	80 kHz	10 MHz ¹⁾
Clock Frequency Register Mode	$1/T_{MAR}$	80 kHz	250 kHz
Acceptable Line Delay	t_{pLine}		indefinite ¹⁾
Acceptable Line Delay Jitter	dt_{pLine}		$\pm 25\% T_{MAS}$

¹⁾ Not limited by the BiSS protocol but due to hardware limitations.

Parameter	Symbol	Slave (required)		Master (recommended)	
		Min	Max	Min	Max
Clock Signal Sensor Mode					
Pulse Width Low	t_{MASl}	25 ns	12.5 μ s	50 ns	6.25 μ s
Pulse Width High	t_{MASh}	25 ns	12.5 μ s	50 ns	6.25 μ s
Clock Signal Register Mode					
Pulse Width Low	t_{MARl}	0.75 μ s	12.5 μ s	1 μ s	9.375 μ s
Pulse Width High	t_{MARh}	0.75 μ s	12.5 μ s	1 μ s	9.375 μ s
PWM Encoding: Pulse Width Difference					
Logic 0 bit: low vs. high duration	$t_{MA0\ l-h}$	1.5 μ s		2 μ s	
Logic 1 bit: high vs. low duration	$t_{MA1\ h-l}$	1.5 μ s		2 μ s	

2. Slave Characteristics

Parameter	Symbol	Min	Max
Timeout Sensor Mode	T_{tos}	12.5 μ s optionally down to 0.5 μ s ²⁾	40 μ s
Timeout Register Mode	T_{tor}	12.5 μ s	40 μ s
Sensor Data Processing Time (delay of start bit output)	t_{busy_s}		40 μ s
Register Data Processing Time	t_{busy_r}		20 ms

After each communication cycle in sensor or register mode the BiSS interface of a slave returns to its idle state where it awaits a new request from the BiSS master. After verifying a certain temporal condition the slave acknowledges the newly set mode and the master drives a new cycle. As opposed to other processes there is thus no permanent monitoring of the temporal condition which would trigger a mode swap with certain frequency conditions on the clock line; instead the desired mode is reactivated using the handshake procedure to increase system security.

The two temporal conditions T_{tos} and T_{tor} (the sensor and register mode timeouts) must be set for a slave's BiSS interface; these determine up to which master clock pause duration the slave retains the selected mode of communication. The master may thus not undershoot a minimum clock frequency. When applying all parameters as listed above sensor mode communication at 80 kHz is always functional for any slave timeout parameters set within the recommended min/max ratings.

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Following the BiSS protocol a slave may request indefinite processing time simply by delaying its start bit. However, it is advisable to limit the count of clock cycles the master issues to allow for secure abortion and error messaging to the controller.

2) Depending on the master's clock frequency a shorter timeout may be used or can be activated dynamically.

3. Data Word Lengths

Data Source	Min	Max
Sensor Data	0 bits	64 bits
Sensor Data CRC Bit Length	0 bits	7 bits
Actor Data (C model protocol only)	0 bits	64 bits
Actor Data CRC Bit Length (C model protocol only)	0 bits	7 bits

4. CRC Polynomials

Recommended CRC Polynomials (CRC bits are sent inverted)	Data Length for Sensor or Actor Data
1011	up to 4 bits
10011	up to 11 bits
100101	up to 26 bits
1000011	up to 57 bits
10001001	up to 64 bits